AMENDMENTS TO THE CLAIMS

Listing of the claims:

Following is a listing of all claims in the present application, which listing supersedes all previously presented claims:

1. (Canceled)

2. (Previously Presented) A sound processor according to claim 3, wherein said bus master means further has a function of determining whether data required in reproduction is stored in said data holding means or not, and acquiring the data from a resource connected to said common bus and storing the data in said data holding means where the data required in reproduction is not stored in said data holding means.

3. (Currently Amended) A sound processor formed on a single semiconductor device to reproduce pulse-code-modulated sound waveform data, comprising:

sequence control means;

bus interface means for a common bus including an address bus and a data bus;

bus master means for issuing an address to said common bus through said bus interface means under control of said sequence control means, and reading and writing data for a resource connected to said common bus;

data holding means for holding part of data read out by said bus master means;

M sets (M being a natural number) of independent digital/analog converting means for converting digital data over a sound channel into an analog sound signal;

data output control means for controlling an output of data to said digital/analog converting means; and

time division multiplexing means for time-division-multiplexing and outputting data of over N sets (N being a natural number greater than 2) of sound channels to each of digital/analog converting means required for reproduction;

whereby data is to be simultaneously reproduced over a plurality of sets of sound channels represented by a product of M and N,

wherein said digital/analog converting means is structured by a plurality of digital/analog converters and said digital/analog converters are in cascade connection, said cascade connection being a connection that an output of each of said digital/analog converters is connected to another one of said digital/analog converters as a reference voltage.

4. (Previously Presented) A sound processor formed on a single semiconductor device to reproduce pulse-code-modulated sound waveform data, comprising:

sequence control means;

bus interface means for a common bus including an address bus and a data bus;

bus master means for issuing an address to said common bus through said bus interface means under control of said sequence control means, and reading and writing data for a resource connected to said common bus;

data holding means for holding part of data read out by said bus master means;

M sets (M being a natural number) of independent digital/analog converting means for converting digital data over a sound channel into an analog sound signal;

data output control means for controlling an output of data to said digital/analog converting means;

time division multiplexing means for time-division-multiplexing and outputting data of over N sets (N being a natural number greater than 2) of sound channels to each of digital/analog converting means required for reproduction,

whereby data is to be simultaneously reproduced over a plurality of sets of sound channels represented by a product of M and N; and

one main volume control digital/analog converter, wherein

each of said M sets of digital/analog converting means is structured by one channel volume control digital/analog converter, one envelope control digital/analog converter, one sound waveform reproducing digital/analog converter and one waveform neutral point outputting digital/analog converter,

said channel volume control digital/analog converters in the number of M being cascade-connected in parallel in a next stage to said main volume control digital/analog converter, in a next stage of which one envelope control digital/analog converter being cascade-connected, in a next stages of which one sound waveform reproducing digital/analog converter and one waveform neutral point outputting digital/analog converter being cascade-connected in parallel, further comprising

first mixing means for mixing outputs of said sound waveform reproducing digital/analog converters in the number of M, and

second mixing means for mixing outputs of said waveform neutral point outputting digital/analog converters in the number of M,

said first and second mixing means having outputs respectively connected to two inputs of a differential amplifier provided at an inside or outside of said semiconductor device.

5. (Previously Presented) A sound processor formed on a single semiconductor device to reproduce pulse-code-modulated sound waveform data, comprising:

sequence control means;

bus interface means for a common bus including an address bus and a data bus;

bus master means for issuing an address to said common bus through said bus interface means under control of said sequence control means, and reading and writing data for a resource connected to said common bus;

data holding means for holding part of data read out by said bus master means;

M sets (M being a natural number) of independent digital/analog converting means for converting digital data over a sound channel into an analog sound signal;

data output control means for controlling an output of data to said digital/analog converting means;

time division multiplexing means for time-division-multiplexing and outputting data of over N sets (N being a natural number greater than 2) of sound channels to each of digital/analog converting means required for reproduction,

whereby data is to be simultaneously reproduced over a plurality of sets of sound channels represented by a product of M and N; and

one main volume control digital/analog converter, wherein

each of said M sets of digital/analog converting means is structured by one channel volume control digital/analog converter, one first envelope control digital/analog converter, one second envelope control digital/analog converter, one first sound waveform reproducing digital/analog converter, one second sound waveform reproducing digital/analog converter, one first waveform neutral point outputting digital/analog converter and one second waveform neutral point outputting digital/analog converter,

said channel volume control digital/analog converters in the number of M being cascade-connected in parallel in a next stage to said main volume control digital/analog converter, in a next stage of which said first envelope control digital/analog converter and said second envelope control digital/analog converter being cascade-connected in parallel, in a next stage to each of said first envelope control digital/analog converters said first sound waveform reproducing digital/analog converter and said first waveform neutral point outputting digital/analog converter each one in number being cascade-connected in parallel, in a next stage to each of said second envelope control digital/analog converters said second sound waveform reproducing digital/analog converter and said second waveform neutral point outputting digital/analog converter each one in number being cascade-connected in parallel, further comprising

first mixing means for mixing outputs of said first sound waveform reproducing digital/analog converters in the number of M, and

second mixing means for mixing outputs of said first waveform neutral point outputting digital/analog converters in the number of M,

third mixing means for mixing outputs of said second sound waveform reproducing digital/analog converters in the number of M, and

fourth mixing means for mixing outputs of said second waveform neutral point outputting digital/analog converters in the number of M,

said first and second mixing means having outputs respectively connected to two inputs of a differential amplifier provided at an inside or outside of said semiconductors,

said third and fourth mixing means having outputs respectively connected to two inputs of a differential amplifier provided at an inside or outside of said semiconductor device.

6. (Previously Presented) A sound processor according to claim 3, wherein said data output control means further has a function to control a constant period of a mute state between adjacent sound channels time-division-multiplexed.

7. (Original) A sound processor according to claim 6, wherein the mute state has a period to be set programmable.

8. (Original) A sound processor according to claim 3, wherein

said data output means further has a function of outputting data in later timing, with respect to timing of outputting data to a certain digital/analog converter, to a digital/analog converter connected in a next stage thereto, and

controlling timing of outputs to eliminate interference between time slots due to signal delay between said cascade-connected digital/analog converters

when outputting data to said cascade-connected digital/analog converter.

9. (Original) A sound processor according to claim 8, wherein said data output control means is to be programmably set in timing of outputting data.

10. (Previously Presented) A sound processor according to claim 3, wherein sound waveform data is configured by two arrays having end codes provided at respective terminal ends of the arrays, and

said bus master means further having a function to start reading at a head of the first array, uninterruptedly starting reading at a head of the second array immediately after reading the end code of the first array, and uninterruptedly starting reading at the head of the second array after reading out the end code of the second array.

11. (Previously Presented) A sound processor according to claim 3, further comprising accumulating means and means for storing pitch control information, wherein

the pitch control information is read out at a constant time interval and

accumulated by said accumulating means, and one part or the whole of an accumulation

result being utilized as address information for access to a common bus of said bus master means.

12. (Previously Presented) A sound processor according to claim 3,

wherein said bus interface means is provided independent for a plurality of common buses.

13. (Previously Presented) A sound processor according to claim 3, further comprising interrupt request control means to be controlled by said sequence control means and generate an interrupt request signal, wherein

said bus master means comprises

waveform reading control means to control reading of sound waveform data,

envelope/preset control means to control reading out of parameters for controlling envelope data and sound reproduction, and

access arbitrating means to arbitrate between an access of from said envelope/preset control means to the common bus and an access of from said waveform reading control means to the common bus,

said bus interface means comprising

first bus interface means to a first common bus, and

second bus interface to a second common bus.

14. (Original) A sound processor apparatus, comprising:

being configured on one single semiconductor device,

first and second buses having independent data transfer capabilities,

a central processing unit and a sound processor according to claim 12 or 13 as bus masters for said first and second buses,

a memory connected to said first bus,

a first bus arbitrating means to administer arbitration over said first bus, and

a second bus arbitrating means to administer arbitration over said second bus.